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09/592,368	06/12/2000	Edouard Bugnion	VMware5	5031

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EXAMINER
SIDDIQI, MOHAMMAD A

ART UNIT	PAPER NUMBER
2126	3

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/592,368	BUGNION, EDOUARD	
	Examiner	Art Unit	
	Mohammad A Siddiqi	2126	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1- 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yates et al. (6549959) (hereinafter Yates) in view of Applicants Admitted Prior Art, Applicants specification pages 1-3.

4. As per independent claim 1,
Yates teaches the invention substantially as claimed:

- Yates teaches in a system in which a hardware target computer system (figure 1A, col 22, lines 15 – 46), which has a target instruction set architecture (ISA)(figure 1A-184, 194, col 22, lines 36-46), executes a target instruction sequence corresponding to a source instruction sequence of a source system (figure 1A, col 22, lines 47-67), which has a source ISA and is running on the target computer

system (figure 1a, col 27, lines 41-49) a method for handling exceptions (figure 3h, 3i, 3j, col 34, lines 45-65) comprising the following steps:

executing the translated target instruction sequence (col 1, lines 60-65).

- sensing the presence of an exception (figure 3a-350,Col 21, lines 22-23); and
- delaying application of the sensed exception until no later than completion (col 31, lines 41-49) of a source instruction corresponding to the translated target instruction sequence being executed at the time of the sensing of the presence of the exception.

Yates fails to disclose converting the source instruction sequence into the target instruction sequence by binary translation each instruction in the source instruction sequence being converted into a corresponding translated target instruction sequence which may consist of a single target instruction;

However, converting the source instruction sequence into the target instruction sequence by binary translation each instruction in the source instruction sequence being converted into a corresponding translated target instruction sequence which may consist of a single target instruction, is well known in the art as it is used for binary translation as evident Applicants Admitted Prior Art on page 1, lines 27-30);

It would have been obvious to one of ordinary skill in the art at the time of invention was made to improve upon exception handler taught by Yates' provides a flexibility to have a single common strategy for processing all exceptions raised during the binary translation either by source or target ISA and execute exception handler on either source ISA or target ISA.

5. As per claim 2, Yates teaches determining beginning and ending addresses of each source instruction and each corresponding translated target instruction (col 80, lines 21-52); and

generating a mapping between the beginning and ending addresses of each source instruction and its corresponding translated target instruction sequence (col 5, lines 8-14).

6. As per claim 3, Yates teaches each exception may be of either of two types -- synchronous and asynchronous (figure 3h, 3j, col 40, lines 24-39) - a synchronous exception being defined as an exception resulting from attempted execution of a target instruction (figure 3j, col 40, lines 24-33)

and an asynchronous exception being defined as an exception resulting from an event unrelated to the execution of a target instruction (figure 3h, 3j, col 38, lines 2-8).

7. As per claim 4 ,Yates teaches a method including step of determining whether each sensed exception is synchronous or asynchronous (figure 3h , 3j, col 40, lines 24-39) .

8. As per claim 5, Yates teaches a method in which synchronous exceptions are of either of two types, namely, transparent (figure 3h,3j, col 34 lines 46-52) and non-transparent (it is implied if an exception is synchronous, and not transparent, then it must be nontransparent exception), a transparent exception being defined as an exception requiring processing action wholly within the target computer system (figure 3h, 3j, col 34 lines 46-52), and a non-transparent exception being defined as an exception requiring processing that alters a visible state of the source system, further including the following steps (figure 3h,3j, col 34 lines 46-52, it is implied if an exception is synchronous, and not transparent, then it must be nontransparent exception):

determining whether the sensed synchronous exception is transparent or nontransparent (figure 3a, 3l);

handling each transparent synchronous exception externally from the source system, the visible state of the source system thereby remaining unaltered (figure 3a – 3l); and

forwarding to the source system for processing each non-transparent synchronous exception (figure 3h , 3j, col 40, lines 24-39).

9. As per claim 6, Yates teaches a method of forwarding each non-transparent synchronous exception (figure eh, 3j, col 34 lines 46-52, it is implied if exception is synchronous and not transparent then it must be nontransparent) to the source system includes the step of converting the sensed exception into a simulated source exception in a source instruction stream, which is sensed by and interrupts the source system (figure 3a, 3l).

10. As per claim 7 Hohensee teaches detecting a method including the following step: upon sensing the presence of an asynchronous exception during execution of a current one of the translated target instruction sequences, delaying processing of the sensed asynchronous exception until completion of the remaining target instructions in the current translated target instruction sequence (figure 2, 3, 4, col 17, lines 14-48). However, does not teach types of exception, an asynchronous exception during execution of a current one of the translated target instruction sequences,

delaying processing of the sensed asynchronous exception until completion of the remaining target instructions in the current translated target instruction sequence.
Yates teaches an asynchronous exception during execution of a current one of the translated target instruction sequences, delaying processing of the sensed asynchronous exception until completion of the remaining target instructions in the current translated target instruction sequence (figure 3h-3l).

11. As per claim 8, Yates teaches a method determining a source instruction pointer as a predetermined function of the final target instruction pointer (figure 3j,col 40, lines 32-48);

forwarding and processing the sensed asynchronous exception (figure 3j,col 40, lines 32-48);

resuming execution at the location in the translation cache that corresponds to a current source instruction pointer (figure 3j,col 40, lines 32-39); and

asynchronous exceptions thereby being processed only upon completion of execution of the translated target instructions corresponding to whole source instructions (col 41, lines 1-27).

12. As per claim 9, Hohensee teaches the delaying processing of the sensed asynchronous exception further includes the step of simulating execution of the remaining target instructions (col 18, lines 44 –67, col 19, lines 1-13).

13. As per claim 10, Yates teaches a method of delaying processing of the sensed exception further includes the step of single-stepping the execution of the remaining target instructions (col 31, lines 41-49).

14. As per claim 11, Yates teaches temporarily replacing with a trap generation instruction the initial target instructions in each of the translated target instruction sequences that correspond to target instruction sequences that possibly immediately follow the current target instruction sequence (fig 4b,col 58, lines 44-67);

resuming execution of the current target instruction sequence from the point at which the asynchronous exception was sensed (figure 3h, 3k, col 43, lines 3-40);

restoring each of the temporarily replaced instructions with their original content after completion of the processing of the sensed asynchronous exception (figure 3h, 3k, col 43, lines 3-40);

upon reaching the trap generation instruction, forwarding and processing the sensed asynchronous exception (figure 3h, 3k).

15. As per claim 12, Yates teaches temporarily replacing with a trap generation instruction each indirect branch instruction, each indirect branch instruction corresponding to a possible last instruction of the current target instruction sequence (fig 4b,col 58, lines 44-67);

resuming execution of the current target instruction sequence from the point at which the asynchronous exception was processed (figure 3h, 3k, col 43, lines 3-40);

restoring each of the temporarily replaced instructions with their original content (figure 3h, 3k, col 43, lines 3-40);

simulating the restored indirect branch instruction (col 56, lines 37-55).

16. As per claim 13, Yates teaches the source system is a virtual machine;

a virtual machine monitor that is operationally installed between the virtual machine and the hardware target computer system, the virtual machine thereby running on the virtual machine monitor (col 3, lines 13-30);

the steps of converting the source instruction sequence into the target instruction sequence by binary translation (col 1, lines 57-65), executing the translated target instruction sequence (col 11, lines 1 –11), sensing the presence of an exception (figure 3a-30), and delaying application of the sensed exception (col 102, lines 1-9), are carried out by the virtual machine monitor (col 101, lines 17-32).

17. As per claim 14, Yates teaches source ISA is identical to the target ISA (col 1, lines 36-65).

18. As per independent claim 15, Yates disclose the invention substantially as claimed:

- Yates teaches in a system in which a hardware target computer system (col 1, lines 14-22), which has a target instruction set architecture (ISA) (col1, lines 36-46), executes a target instruction sequence corresponding to a source instruction sequence of a source system (col1, lines 11-13), which has a source ISA and is running on the target computer system (col 1, lines 13-25), a method for handling exceptions comprising the following steps:
- converting the source instruction sequence into the target instruction sequence by binary translation, each instruction in the source

instruction sequence being converted into a corresponding translated target instruction sequence (col 1, lines 13-25, which may consist of a single target instruction (col1, lines 60-65);

- executing the translated target instruction sequence (col 1, lines 60-65;

sensing the presence of an exception (figure 3a-350,Col 21, lines 22-23),

- each exception being of either of two types -- synchronous and asynchronous - a synchronous exception being defined as an exception resulting from attempted execution of a target instruction and an asynchronous exception is defined as an exception resulting from an event unrelated to the execution of a target instruction (figure 3h, 3j, col 40,lines 24-39),
- synchronous exceptions being of either of two types, namely, transparent (figure 3a-3f, col 34, lines 46-52) and non-transparent (it is implied if an exception is synchronous, and not transparent, must be nontransparent exception), a transparent exception being defined as an exception requiring processing action wholly within the target computer system (figure 3a-3f, col 34, lines 46-52), and a non-transparent exception being defined as an exception requiring processing that alters a visible state of the source system(figure 3h, 3j, col 34, lines 24-39);
- determining whether each sensed exception is synchronous or asynchronous (figure 3a-3l);
- determining whether each sensed synchronous exception is transparent or non transparent (figure 3h,3j, col 34 lines 46-52, it is implied if an exception is synchronous, and not transparent, then it must be nontransparent exception);
- upon sensing the presence of an asynchronous exception during execution of a current one of the translated target instruction sequences (figure 3h, 3j, col 40, lines 24-39), delaying processing of the sensed asynchronous exception until completion of the remaining target instructions in the current translated target instruction sequence (col 102, lines 17-32);
- determining beginning and ending addresses of each source instruction and each corresponding translated target instruction (col 80, lines 21-52);
- generating a mapping between the beginning and ending addresses of each source instruction and its corresponding translated target instruction sequence (col 5, lines 8-23);

- handling each transparent synchronous exception externally from the source system, the visible state of the source system thereby remaining unaltered (figure 3h, 3j, col 40, lines 24-39);
- forwarding to the source system for processing each non-transparent
- synchronous exception (figure 3a –30);
- determining a source instruction pointer as a predetermined function of the final target instruction pointer (figure 1a-602, col 22, lines 56-67));
- forwarding and processing each sensed asynchronous exception (figure 3h, 3j, col 40, lines 24-39);
- resuming execution at the location in the translation cache that corresponds to a current source instruction pointer (figure 3h, 3k, col 43, lines 3-40), asynchronous exceptions thereby being processed only upon completion of execution of the translated target instructions corresponding to whole source instructions (figure 3h, 3k, col 43, lines 3-40);
- delaying application of the sensed exception until no later than completion of a source instruction corresponding to the translated target instruction sequence being executed at the time of the sensing of the presence of the exception (figure 3a-3o, col 11, lines 1-11);

in which:

- the source system is a virtual machine (col1, lines 35-65);
- a virtual machine monitor that is operationally installed between the virtual machine and the hardware target computer system , the virtual machine thereby running on the virtual machine monitor (figure 1a, col 3, lines 13-30); and
- the steps of converting the source instruction sequence into the target instruction sequence by binary translation (col1, lines 57065), executing the translated target instruction sequence (col 11, lines 1-11), sensing the presence of an exception (figure 3a-30), and delaying application of the sensed exception (col 102, lines 1-9), are carried out by the virtual machine monitor (col 101, lines 17-32.

Yates fails to disclose converting the source instruction sequence into the target instruction sequence by binary translation each instruction in the source instruction sequence being converted into a corresponding translated target instruction sequence which may consist of a single target instruction;

However, converting the source instruction sequence into the target instruction sequence by binary translation each instruction in the source instruction sequence being converted into a corresponding translated target instruction sequence which may consist of a single target instruction, is well

known in the art as it is used for binary translation as evident Applicants Admitted Prior Art on page 1, lines 27-30);

It would have been obvious to one of ordinary skill in the art at the time of invention was made to improve upon exception handler taught by Yates' provides a flexibility to have a single common strategy for processing all exceptions raised during the binary translation either by source or target ISA and execute exception handler on either source ISA or target ISA.

19. As per independent claim 16, it is rejected for the similar reason as stated in claim 1.

20. A system as in claim 17, it is rejected for the similar reason as stated in claim 2.

21. As per claim 18, it is rejected for the similar reason as stated in claims 3 and 4.

22. As per claim 19, it is rejected for the similar reason as stated in claim 5.

23. As per claim 20, it is rejected for the similar reason as stated in claim 9.

24. As per claim 21, it is rejected for the similar reason as stated in claim 10.

25. As per claim 22, it is rejected for the similar reason as stated in claim

11.

26. As per claim 23, it is rejected for the similar reason as stated in claim 13.

27. As per claim 24, it is rejected for the similar reason as stated in claim 14.

28. The prior art made of record and not relied upon is considered

pertinent to applicant's disclosure:

a. Hohensee U.S. 5,778,211

c. Hookway U.S. 5842017

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad A Siddiqi whose telephone number is (703) 305-0353. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MAS

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100